11/06/00 U.S. PTO

11.08.00

Jc813 U.S. PTO
09/707521
11/06/00

Attorney Docket No.: SONY-50P3845

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

I hereby certify that this transmittal of the below described documents is being deposited with the United States Postal Service in an envelope bearing Express Mail Postage and an Express Mail label, with the below serial number, addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.			
Express Mail Label No.:	EL709925563US	Name of Person Making the Deposit:	ANTHONY CHOU
Date of Deposit:	11/06/00	Signature of the Person Making the Deposit:	Anthony Chou

Inventor(s): Amelia C. Luna and Jason (Naxin) Wang

Title: IMPLEMENTATION OF A DV VIDEO DECODER WITH A VLIW PROCESSOR AND A VARIABLE LENGTH DECODING UNIT

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Transmittal of a Patent Application
(Under 37 CFR §1.53)

Transmitted herewith is the above identified patent application, including:

X Specification, claims and abstract, totaling 41 pages.
__ Formal drawings, totaling __ pages.
X Informal drawings, totaling 6 pages.
X Declaration and Power of Attorney.
__ Information Disclosure statement.
__ Form 1449
X Assignment(s)
X Assignment Recordation Form (duplicate)
__ Preliminary Amendment
__
__ Other: __

FEES DUE

The fees due for filing the specification pursuant to 37 C.F.R. § 1.16 and for recording of the Assignment, if any, are determined as follows:

CLAIMS					
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	FEES
Basic Application Fee					$710.00
Total Claims	37	Minus 20=	17	X $18 =	$306.00
Independent Claims	4	Minus 3=	1	X $80=	$80.00
If multiple dependent claims are presented, add $260.00					$0.00
Add Assignment Recording Fee of $40.00 If Assignment document is enclosed					$40.00
TOTAL APPLICATION FEE DUE					$1,136.00

PAYMENT OF FEES

The full fee due in connection with this communication is provided as follows:

1. Not enclosed

   [ ] No filing fee is to be paid at this time.

2. Enclosed

   [X] Filing fee

   [X] Recording assignment

   [ ] Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached

   [ ] For processing an application with specification in a non-English language

   [ ] Processing and retention fee

   [ ] Fee for international-type search report

   [X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085. A duplicate copy of this authorization is enclosed.

   [X] A check in the amount of $1,136.00

   [ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

This application is filed pursuant to 37 C.F.R. § 1.53 in the name of the above-identified Inventor(s).

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

[X] This transmittal ends with this page.

Respectfully submitted,

Date: November 6, 2000

By: Jose S. Garcia
Jose S. Garcia
Reg. No. 43,628

SONY-50P3845/ACM/JSG

United States Patent Application

For

IMPLEMENTATION OF A DV VIDEO DECODER WITH A VLIW PROCESSOR AND A VARIABLE LENGTH DECODING UNIT

Inventors:

Amelia C. Luna

Jason (Naxin) Wang

Prepared by:

WAGNER, MURABITO & HAO LLP

Two North Market Street

Third Floor

San Jose, California 95113

(408) 938-9060

IMPLEMENTATION OF A DV VIDEO DECODER WITH A VLIW PROCESSOR AND A VARIABLE LENGTH DECODING UNIT

RELATED U.S. APPLICATION

This patent application claims the benefit of U.S. Provisional Application No. 60/176,256, filed on January 15, 2000, entitled "PRE-PARSING OF VARIABLE LENGTH DIGITAL VIDEO (DV) STREAMS", by Amelia C. Luna, and Jason (Naxin) Wang.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention generally relates to the field of digital video data processing. More particularly, the present invention relates to the field of decoders for decoding digital video data.

RELATED ART

The advent of fast and powerful electronic circuits has enabled the development of digital video systems (e.g., digital cameras, digital VCR's, etc.). These digital video systems offer high resolution and high quality recorded images, surpassing the resolution and quality provided by analog video systems (e.g., analog cameras, analog VCR's, etc.). Moreover, the digital video systems include digital video data as well as digital audio data, raising the entertainment experience of the user. Since digital video systems manipulate digital data, the original recorded images stored in

the digital format of digital video systems do not suffer the deterioration in quality observed with the original recorded images stored in the analog format of analog video systems.

Some digital video systems have been integrated into a computer system, allowing a user to edit and to view digital video data and digital audio data. Other digital video systems have been designed to communicate and to transfer digital data (e.g., digital video data and digital audio data) to a computer system, permitting the user to exchange or to view the digital data.

A popular digital video system stores digital video data which is formatted as specified in a specification entitled, "The Specification of Consumer Use Digital VCR's using 6.3mm Magnetic Tape", (HD Video Conference, December, 1994). This specification is commonly known as the DV standard. The DV standard is a compressed digital video data and digital audio data recording standard. A DV digital video system uses a 1/4 inch (6.35mm) metal evaporate tape to record very high quality digital video data. Alternatively, a DV digital video system can record by transmitting to a memory device (e.g., hard drive, RAM, ROM, etc.) very high quality digital video data and digital audio data for storing therein. Both consumers and professionals use DV digital video systems.

To play the digital video data which is formatted according to the DV standard, the DV digital video system includes a DV video decoder for processing the digital

video data into a format which can be displayed on an electronic display device. Since the DV video decoder processes the digital video data in real-time, speed and performance are crucial characteristics of the DV decoder. Generally, speed and performance are achieved at great cost. Hardware and software specifically designed for the DV video decoder can price the DV digital video system out of reach of the average consumer. Typically, off-the-shelve hardware and software adapted for the DV video decoder does not provide the speed and performance necessary for a DV digital video system. Some equipment manufactures have designed general-purpose components to provide a software solution for manufacturing low cost consumer digital video decoders.

SUMMARY OF THE INVENTION

A decoder for decoding a plurality of digital video data is described. In an embodiment, the decoder comprises a DV video decoder for decoding digital video data which is formatted according to the DV standard. The DV video decoder has a Very-Long Instruction Word (VLIW) processor and a variable length decoding unit. The VLIW processor includes a preparser unit for recovering a decoding order of the digital video data so that the variable length decoding unit can process the digital video data. The variable length decoding unit decodes a variable length coding format of the digital video data which has been preparsed by the VLIW processor. Furthermore, the VLIW processor includes a decompression unit for decompressing the digital video data which has been decoded by the variable length decoding unit. In an embodiment, the VLIW processor and the variable length decoding unit are formed on the same semiconductor device.

The decoder of the present invention primarily utilizes software to process the digital video data. Because the decoder is implemented in software, the decoder can be adapted to process different types of data formats simply by modifying the software rather than designing a new decoder.

The digital video data has an arrangement specified by the DV standard. In this arrangement, the digital video data is grouped into a plurality of Discrete Cosine Transform (DCT) blocks of fixed length representing compressed and variable length coded digital video data for a fixed number of pixels. During the DV recording

process, the fixed number of pixels may generate more digital video data than can be stored within the fixed length of a particular DCT block. Since each DCT block has a fixed length, some of the digital video data belonging to the particular DCT block is distributed to one or more additional DCT blocks having unused space within their fixed lengths.

The VLIW processor preparses the digital video data so that the digital video data is re-associated with the corresponding DCT block. After the VLIW processor has prepared the digital video data, the digital video data is contiguous within the corresponding DCT block. Thus, the DCT blocks are transformed from fixed length to variable length to accommodate all the digital video data belonging to each DCT block. In addition, the re-ordering of the digital video data within the DCT block structure enables the variable length decoding unit to decode a variable length coding format of the digital video data. According to the present invention, the logically complicated process of preparsing the digital video data is executed by the VLIW processor while the variable length decoding unit focuses on decoding variable length symbols of the digital video data. Since the variable length decoding unit is designed to perform variable length decoding, the variable length decoding unit usually does not have enough processing logic (e.g., circuitry or software code) to collect the extra bits of a particular DCT block that are stored in other DCT blocks' unused space.

Moreover, a first plurality of digital video data can be preparsed by the VLIW processor while the variable length decoder unit decodes a second plurality of digital

video data which has been preparsed. Additionally, the second plurality of digital video data which has been preparsed can be decoded by the variable length decoder unit while the VLIW processor decompresses a third plurality of digital video data which has been decoded. Since the DV decoder of the present invention concurrently executes multiple operations on the digital video data, the DV decoder of the present invention features superior speed and performance characteristics while containing costs.

These and other advantages of the present invention will no doubt become apparent to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the drawing figures.

In one embodiment, the present invention includes a method of processing digital video data for displaying, the method comprising the steps of: a) preparsing the digital video data to recover a decoding order of the digital video data; b) decoding a variable length coding format of the digital video data; c) moving the digital video data that has been processed by the step b); and d) decompressing the digital video data to facilitate displaying the digital video data on an electronic display device.

In another embodiment, the present invention includes an apparatus for processing digital video data for displaying, the apparatus comprising: a processor configured to preparse the digital video data to recover a decoding order of the digital video data; and a variable length decoding unit coupled to the processor, wherein the

variable length decoding unit is configured to decode a variable length coding format of the digital video data.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the present invention.

Figure 1A illustrates a digital video system in which embodiments of the present invention can be practiced.

Figure 1B illustrates encoding steps for the digital video data on which embodiments of the present invention can be practiced.

Figure 2 illustrates a frame of digital video data on which embodiments of the present invention can be practiced.

Figure 3 illustrates a segment of digital video data on which embodiments of the present invention can be practiced.

Figure 4 illustrates a macro block of digital video data on which embodiments of the present invention can be practiced.

Figure 5 illustrates a DCT block of digital video data on which embodiments of the present invention can be practiced.

Figure 6 illustrates a decoder, showing a VLIW processor and a variable length decoder unit in accordance with an embodiment of the present invention.

Figure 7 illustrates operations executed on digital video data by the decoder of Figure 6 in accordance with an embodiment of the present invention.

Figure 8 illustrates a recovered data buffer in accordance with an embodiment of the present invention.

Figure 9 illustrates a decoded data buffer in accordance with an embodiment of the present invention.

The drawings referred to in this description should not be understood as being drawn to scale except if specifically noted.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

NOTATION AND NOMENCLATURE

Some portions of the detailed descriptions which follow are presented in terms of procedures, logic blocks, processing, and other symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. In the present application, a procedure, logic block, process, etc., is conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are

those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. It has proved convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as "preparsing", "decoding", "decompressing", "de-shuffling" or the like, refer to the actions and processes of an electronic system or a computer system. The computer system or similar electronic computing device manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other information storage, transmission, or display devices.

DV VIDEO DECODER

Figure 1A illustrates a digital video system 50 in which embodiments of the present invention can be practiced. Although the description will focus on digital video data which is formatted as specified in a specification entitled, "The Specification of

Consumer Use Digital VCR's using 6.3mm Magnetic Tape", (HD Video Conference, December, 1994), commonly known as the DV standard, it should be understood that the present invention is applicable to digital video data which is formatted in accordance with other standards, such as standards developed by the Moving Picture Experts Group (MPEG) (e.g., MPEG-1, MPEG-2, MPEG-3, etc.).

In an embodiment, a DV data source 80 is coupled to the digital video system 50 via a data bus 85. The DV data source 80 stores the recorded DV data. The DV data source 80 can be a DV tape, a DV disk, a memory device (e.g., hard drive, RAM, ROM, etc.), or any other storage device which is capable of storing DV data. In an embodiment, the data bus 85 comprises a IEEE 1394 serial data bus 85 which is a low-cost and high-performance digital bi-directional serial bus. Alternatively, the data bus 85 can be implemented as any other type of data bus. The DV data is organized into the digital interface format (DIF) for digital transmission via the IEEE serial data bus 85.

In an embodiment, the digital video system 50 comprises a DIF parser 90 coupled to the data bus 85, a digital video data decoder 100 coupled to the DIF parser 90, and a digital audio data decoder 110 coupled to the DIF parser 90. The DIF parser 90 receives the DV data from the DV data source 80 via the data bus 85. The DIF parser 90 separates the DV data into a plurality of data streams. The data streams include a first data stream of digital video data which is formatted according to the DV standard and a second stream of digital audio data which is formatted according to the

DV standard. It should be understood that the DV data can include other data, such as subcode, auxiliary video data, or auxiliary audio data. It should be understood that the DIF parser 90 can separate the DV data into other data streams, such as a data stream for subcode data (e.g., error correction data, timecode data, etc.).

In an embodiment, the digital video data decoder 100 receives the stream of digital video data, which is formatted according to the DV standard, from the DIF parser 90 via the data path 93. Similarly, the digital audio data decoder 110 receives the stream of digital audio data, which is formatted according to the DV standard, from the DIF parser 90 via the data path 96.

In an embodiment, the digital video data decoder 100 comprises a DV video decoder 100. The DV video decoder 100 decodes the digital video data into a format for displaying the recorded images on an electronic display device 120 coupled to the digital video system 50. From the DV video decoder 100, the digital video data is moved to the electronic display device 120 via a data path 105. The operation of the DV video decoder 100 will be described below. The stream of digital video data received by the DV video decoder 100 arrives in a compressed and variable length coded format compliant with the DV standard. As will be discussed below, the DV video decoder 100 decodes the variable length code format of the digital video data and decompresses the digital video data.

The digital audio decoder 110 comprises a DV audio decoder 110. The DV audio decoder 110 decodes the digital audio data into a format for rendering on a sound device 130 coupled to the digital video system 50 (e.g., a DV system). From the DV audio decoder 110, the digital audio data is moved to the sound device 130 via a data path 115. The sound device 130 can be implemented in any manner. For example, the sound device 130 can include a sound amplifier and a speaker.

It should be understood that the digital video system 50 (e.g., a DV system) of Figure 1A can be configured in any other manner.

Figure 1B illustrates encoding steps for the digital video data on which embodiments of the present invention can be practiced. Although the discussion will focus on the DV standard, it should be understood that the present invention can be practiced with digital video data which is formatted according to other standards (e.g., MPEG-1, MPEG-2, MPEG-3, etc.).

Before beginning the process of encoding digital video data into the DV format, analog video data is converted into digital video data comprising data in the Y,Cr,Cb color space, whereas Y refers to luminance data while Cr and Cb refer to chrominance data. If the analog video data is sampled according to the Phase Alternation Line (PAL) or (625/50) TV standard, the digital video data comprises data in the Y,Cr,Cb 4:2:0 color space. If the analog video data is sampled according to the National Television System

Committee (NTSC) or (525/60) TV standard, the digital video data comprises data in the Y,Cr,Cb 4:1:1 color space.

In an embodiment of the encoding procedure, a stream of digital video data (e.g., data in the Y,Cr,Cb color space) first proceeds to the shuffling process 210. Here, the digital video data is divided into a plurality of macro blocks. The macro blocks are shuffled, or moved around. The shuffling step minimizes the effect of contiguous errors on the appearance of a frame of digital video data. Additionally, the shuffling step aids in error correction, makes error concealment more effective, and evens out the distribution of digital video data in a frame so that there is an even flow of digital video data through the rest of the encoding steps.

The stream of digital video data proceeds to the DCT process 220. Here, the digital video data is compressed using the Discrete Cosine Transform (DCT). In particular, digital video data is divided into a plurality of DCT blocks comprising the digital video data of 8 x 8 pixels and then the DCT blocks are compressed using DCT. In the 8-8-DCT mode, the digital video data of 8 x 8 pixels are compressed as a block. In the 2-4-8-DCT mode, the digital video data of 8 x 8 pixels are deinterlaced into two independent blocks comprising the digital video data of 4 x 8 pixels. Moreover, each block of digital video data of 4 x 8 pixels is compressed using DCT. The DCT process 220 generates DC coefficients and AC coefficients which are stored in each DCT block of digital video data.

The stream of digital video data proceeds to the quantization process 230. Here, the digital video data (e.g., DC coefficients and AC coefficients) compressed by the DCT process 220 is further compressed by being mapped to quantization intervals.

The stream of digital video data proceeds to the variable length coding process 240. Here, the AC coefficients of the digital video data are encoded by a variable length coding algorithm. In an embodiment, the variable length coding algorithm comprises a Huffman code format. According to the Huffman code format, a variable length coding table assigns variable length codes or symbols to AC coefficient of the digital video data, whereas the variable length symbols are shorter for more common AC coefficients and are longer for less common AC coefficients.

It should be understood that hardware or software can be used in implementing the shuffling process 210, the DCT process 220, the quantization process, and the variable length coding process 240. Moreover, the digital video data can be encoded into the DV standard using other processes.

After performing the encoding steps of Figure 1B on the digital video data, the digital video data is stored in a DV tape, a DV disk, a memory device (e.g., hard drive, RAM, ROM, etc.), or any other storage device which is capable of storing DV data. The digital video data (which is now compressed and variable length coded) is stored in the arrangement illustrated in Figures 2-5.

Figure 2 illustrates a frame 250 of digital video data (compressed and variable length coded as illustrated in Figure 1B) on which embodiments of the present invention can be practiced. The digital video data encoded into the DV standard is divided into a plurality of frames. Each frame 250 includes a plurality of segments 251- 257 of digital video data. As illustrated in Figure 2, the frame 250 includes 270 separate segments. It should be understood that the number of segments depends on the TV standard used in sampling the analog video data as discussed above. The NTSC TV standard generally requires 270 segments per frame of digital video data.

Figure 3 illustrates a segment 350 of digital video data (compressed and variable length coded as illustrated in Figure 1B) on which embodiments of the present invention can be practiced. The segment 350 includes a plurality of macro blocks 351-355 of digital video data. Here, the segment 350 has five macro blocks of digital video data. It should be understood that each segment of Figure 2 is arranged as illustrated in Figure 3.

Figure 4 illustrates a macro block 450 of digital video data (compressed and variable length coded as illustrated in Figure 1B) on which embodiments of the present invention can be practiced. The macro block 450 includes a Macro Block (MB) header 451A, and a plurality of DCT blocks 451-456. In an embodiment, the MB header 451A includes four bits for STA (status of the compressed macro block) and four bits for the QNO (quantization number applied to the macro block). Here, the macro block 450 includes six DCT blocks of digital video data. DCT blocks 451-454 include digital video

data corresponding to luminance data of the recorded images. DCT blocks 455-456 include digital video data corresponding to chrominance data of the recorded images. It should be understood that each macro block of Figure 3 is arranged as illustrated in Figure 4.

Figure 5 illustrates a DCT block 550 of digital video data (compressed and variable length coded as illustrated in Figure 1B) on which embodiments of the present invention can be practiced. The DCT block 550 includes a plurality of digital video data. In an embodiment, the DCT block 550 includes a motion bit 557A which indicates whether to perform 8-8 IDCT or 2-4-8 IDCT, a class number 557B which is used for quantization, a plurality of DC coefficients 551 which are compressed as described in connection with Figure 1B, a plurality of AC coefficients 552 which are compressed and variable length coded as described in connection with Figure 1B, and an unused space/overflow AC coefficients 554. The DCT block 550 can include an end-of-block code (EOB) 553, which is variable length coded, to indicate the end of the AC coefficients corresponding to the DCT block. The DCT computation discussed in connection with Figure 1B generates the DC coefficients and the AC coefficients for each DCT block of digital video data of 8 x 8 pixels. In an embodiment, the DC coefficients 551 area has a total length of nine bits, the motion bit 557A has a length of one bit, and the class number 557B has a length of two bits. It should be understood that each DCT block of Figure 4 is arranged as illustrated in Figure 5.

Moreover, each DCT block illustrated in Figures 4-5 is allocated a fixed length of bits or bytes of digital video data as required by the DV standard. The number of bits or bytes required to store the AC coefficients of the digital video data of 8 x 8 pixels may vary widely in accordance with the quantization process 230 described with respect to Figure 1B. A particular DCT block may have unused space 554 within its fixed length allocation of bits or bytes while another DCT block may not have sufficient space within its fixed length allocation of bits or bytes for the AC coefficients of the digital video data of 8 x 8 pixels, thus generating overflow AC coefficients. The overflow AC coefficients are distributed to DCT blocks (within the same macro block) having unused space 554. The remaining overflow AC coefficients are distributed to DCT blocks (within the same segment) having unused space 554. Thus, unused space 554 in a DCT block may be used to store overflow AC coefficients belonging to other DCT blocks within the same macro block, or even within the same segment.

It should be understood that the frame 250, the segment 350, the macro block 450, and the DCT block 550 illustrated in Figures 2-5 can have additional types of data. Moreover, it should be understood that the digital video data can be arranged in a manner other than that described with respect to Figures 2-5.

Figure 6 illustrates a video decoder 100 of Figure 1A, showing a VLIW processor 610 and a variable length decoder unit 620 in accordance with an embodiment of the present invention. Although the stream of digital video data decoded by the video decoder 100 is formatted according to the DV standard, it should

be understood that the video decoder 100 of the present invention can decode digital video data formatted according to other standards (e.g., MPEG-1, MPEG-2, MPEG-3, etc.).

The video decoder 100 of the present invention primarily utilizes software to process the digital video data. Because the video decoder is implemented in software, the video decoder can be adapted to process different types of data formats simply by modifying the software rather than designing a new video decoder.

In an embodiment, the video decoder 100 (e.g., a DV video decoder) includes a digital video data buffer 660, a Very-Long Instruction Word (VLIW) processor 610 coupled to the digital video data buffer via a data path 665, a variable length decoder unit 620 coupled to the VLIW processor 610, and a frame buffer 670 coupled to the VLIW processor 610 via a data path 675. In an embodiment, the VLIW processor 610 and the variable length decoder unit 620 are formed on the same semiconductor device such that the VLIW processor 610 functions as the main or core processor while the variable length decoder unit 620 functions as a coprocessor. Since the digital video data is formatted according to the DV standard, the video decoder 100 will be referred to as the DV video decoder 100. The DV video decoder 100 executes on the digital video data (compressed and variable length coded) the inverse of the encoding steps discussed with respect to Figure 1B in order to display the digital video data on an electronic display device 120 (Figure 1A). In particular, the DV video decoder 100 decodes the variable length symbols of the digital video data,

decompresses the digital video data by performing an inverse quantization process, decompresses the digital video data by performing an inverse discrete cosine transform (IDCT) process, and de-shuffles the digital video data.

In Figure 6, some of the data paths may be logical rather than physical (e.g., a data bus). In addition, some of the data paths may share one or more data buses.

The processing of the digital video data (compressed and variable length coded as illustrated in Figure 1B) is executed on the VLIW processor 610 and on the variable length decoder unit 620. The VLIW processor 610 preparses the digital video data to recover a decoding order of the digital video data by re-associating the overflow AC coefficients (compressed and variable length coded) of the digital video data with the corresponding DCT block, generating digital video data that is contiguous within the corresponding DCT block. In particular, a preparser unit 640 of the VLIW processor 610 preparses the digital video data. The DCT blocks are transformed from fixed length to variable length to accommodate all the digital video data belonging to each DCT block. Once the digital video data is arranged in the decoding order, the variable length coding format of the digital video data which has been preparsed can be decoded by the variable length decoder unit 620. Furthermore, the VLIW processor 610 decompresses the digital video data which has been decoded and de-shuffles the digital video data which has been decompressed. In particular, a decompression unit 630 of the VLIW processor 610 decompresses and de-shuffles the digital video data.

The DV video decoder 100 of the present invention has superior speed and performance characteristics because the VLIW processor 610 preparses the digital video data prior to the variable length decoder unit 620 decoding the digital video data. The VLIW processor 610 breaks program instructions down into basic operations that can be performed in parallel. Complexity is moved from the hardware of the VLIW processor 610 to software executed by the VLIW processor 610. The variable length decoder unit 620 can decode variable length symbols much faster than the VLIW processor 610. However, it is very difficult to use the variable length decoder unit 620 to preparse the digital video data to recover the decoding order of the digital video data so that the digital video data is contiguous within the corresponding DCT block since the variable length decoder unit 620 lacks the general functionality of a general purpose processor or the VLIW processor 610.

According to the present invention, the logically complicated process of preparsing the digital video data is executed by the VLIW processor 610, leaving the variable length decoder unit 620 responsible for decoding the variable length symbols of the digital video data which has been preparsed. Moreover, the VLIW processor 610/variable length decoder unit 620 architecture facilitates concurrent execution of multiple processes to improve performance of the DV video decoder 100. A first plurality of digital video data is preparsed by the preparser unit 640 while a second plurality of digital video data which has been preparsed is decoded by the variable length decoder unit 620. Moreover, a third plurality of digital video data which has been decoded is decompressed and de-shuffled while the second plurality of digital

video data which has been preparsed is decoded by the variable length decoder unit 620.

Referring to Figure 6, a stream of digital video data is received by the digital video data buffer 660. Digital video data is transferred to the preparser unit 640 via the data path 665. After the preparser unit 640 processes the digital video data, the digital video data proceeds to the variable length decoder unit 620. From the variable length decoder unit 620, the digital video data proceeds to the decompression unit 630. Finally, the digital video data is transferred via the data path 675 from the decompression unit 630 to the frame buffer 670 from which the digital video data can be readily displayed on an electronic display device 120 (Figure 1A). In an embodiment, the digital video data buffer 660 and the VLIW processor 610 are formed on separate semiconductor devices. The digital video data buffer 660 can be implemented as synchronous dynamic random access memory (SDRAM) or any other type of memory. In an embodiment, the frame buffer 670 and the VLIW processor 610 are formed on separate semiconductor devices.

In an embodiment, the VLIW processor 610 comprises a model MAP1000A media accelerated processor manufactured by Equator Technologies, Inc. of Seattle, WA (www.equator.com). The preparser unit 640 and the decompression unit 630 are implemented on the VLIW processor 610 or core processor of the MAP1000A. The variable length decoder unit 620 is implemented on the coprocessor (which includes a variable length encoder/decoder) of the MAP1000A. It should be understood the DV

video decoder 100 can be implemented with other VLIW processors or general purpose processors.

Figure 7 illustrates operations executed on digital video data by the DV video decoder 100 of Figure 6 in accordance with an embodiment of the present invention. A data streamer 705 of the VLIW processor 610 is coupled to the digital video data buffer 660 and to a data segment buffer 710. In an embodiment, the data streamer 705 comprises a programmable direct memory access (DMA) unit. The data streamer 705 moves the digital video data to the preparser unit 640. In particular, the data streamer 705 moves the digital video data to the data segment buffer 710. In an embodiment, the data streamer 705 moves a segment of digital video data or five macro blocks of digital video data or 30 DCT blocks of digital video data to the data segment buffer 710. It should be understood that the amount of digital video data transferred to the data segment buffer 710 depends on the size of the data segment buffer 710. In an embodiment, the data segment buffer 710 comprises static random access memory (SRAM).

The data segment buffer 710 is coupled to a de-framing pass 1 unit 720 of the VLIW processor 610. The de-framing pass 1 unit 720 of the VLIW processor 610 executes software instructions which determine those DCT blocks in which all the AC coefficients (compressed and variable length coded) are stored within the corresponding DCT blocks. An EOB 553 (Figure 5), which is variable length coded, found before the end of the fixed length of the DCT block indicates that the DCT block

stores all of its DC coefficients (compressed) and AC coefficients (compressed and variable length coded). In an embodiment, 30 DCT blocks of digital video data are processed in parallel by the de-framing pass 1 unit 720 of the VLIW processor 610. It should be understood that the number of DCT blocks which can be processed in parallel depends on the processing speed of the preparser unit 640 and the resources allocated by the VLIW processor 610. The de-framing pass 1 unit 720 of the VLIW processor 610 is coupled to a recovered buffer 750 and a data overflow buffer 730.

The DCT blocks of digital video data having overflow AC coefficients (compressed and variable length coded) are moved from the de-framing pass 1 unit 720 to the data overflow buffer 730 while the rest of the DCT blocks are moved from the de-framing pass 1 unit 720 to the recovered buffer 750. The data overflow buffer 730 is coupled to a de-framing pass 2 & 3 unit 740 of the VLIW processor 610. From the data overflow buffer 730, the DCT blocks of digital video data having overflow AC coefficients (compressed and variable length coded) are moved to a de-framing pass 2 & 3 unit 740 of the VLIW processor 610. The de-framing pass 2 & 3 unit 740 of the VLIW processor 610 executes software instructions which re-associate the overflow AC coefficients (compressed and variable length coded) belonging to DCT blocks within the same macro block. Moreover, the de-framing pass 2 & 3 unit 740 of the VLIW processor 610 executes software instructions which re-associate the overflow AC coefficients (compressed and variable length coded) belonging to DCT blocks within the same segment. The de-framing pass 2 & 3 unit 740 of the VLIW processor 610 is coupled to the recovered data buffer 750. From the de-framing pass 2 & 3 unit

740 of the VLIW processor 610, the DCT blocks are moved to the recovered data buffer 750.

After processing by the de-framing pass 1 unit 720 of the VLIW processor 610 and the de-framing pass 2 & 3 unit 740 of the VLIW processor 610, the preparser unit 640 has recovered a decoding order of the digital video data so that the variable length decoder unit 620 can decode the digital video data. The recovered data buffer 750 stores digital video data that is contiguous within the corresponding DCT block. The overflow AC coefficients (compressed and variable length coded) are now associated with the corresponding DCT block. The DCT blocks have variable lengths to accommodate all the overflow AC coefficients (compressed and variable length coded) belonging to the corresponding DCT block. Additionally, each DCT block includes an EOB symbol to indicate the end of the DC coefficients (compressed) and the AC coefficients (compressed and variable length coded) of the DCT block. If there is no EOB symbol within a DCT block in the input stream of digital video data received from the digital video data buffer 660, the de-framing pass 2 & 3 unit 740 inserts an EOB symbol within the end of that DCT block. Therefore, the variable length decoding unit 620 can determine the end of each DCT block by looking for the EOB symbol. Moreover, the variable length decoder unit 620 can now proceed to decode the variable length code format of the DCT blocks of digital video data. As discussed above, it is very difficult to utilize the variable length decoder unit 620 to preparse the digital video data. In an embodiment, the variable length code format comprises a Huffman code format.

The data streamer 705 transfers the digital video data from the recovered data buffer 750 to a get bit unit 755 of the variable length decoder unit 620. The get bit unit 755 is coupled to a programmable variable length encoder/decoder 760. The programmable variable length encoder/decoder 760 is coupled to a memory buffer 765.

In an embodiment, the get bit unit 755 comprises hardware that facilitates movement of digital video data from the data streamer 705 to the programmable variable length encoder/decoder 760. In an embodiment, the programmable variable length encoder/decoder 760 executes firmware instructions which decode the variable length symbols of the AC coefficients of the digital video data. The variable length symbols are Huffman code symbols. In an embodiment, the variable length decoder unit 620 decodes the variable length code format of a DCT block of digital video data at a time. Moreover, the programmable variable length encoder/decoder 760 controls how the digital video data is transferred by the data streamer 705 and by the get bit unit 755 during the variable length decoding process. The memory buffer 765 stores DCT blocks of digital video data that have been decoded by the programmable variable length encoder/decoder 760.

The data streamer 705 transfers the digital video data from the memory buffer 765 to a decoded data buffer 770 of a decompression unit 630 of the VLIW processor 610. The decoded data buffer 770 is coupled to a IDCT & IQ unit 775 of the VLIW

processor 610. The IDCT & IQ unit 775 of the VLIW processor is coupled to the data streamer 705. A de-shuffling unit 780 is coupled to the data streamer 705.

The preparser unit 640 and the decompression unit 630 can be executed on the same VLIW processor 610. In an embodiment, the preparser unit 640 and the decompression unit 630 may run or execute according to time share criteria. For example, the preparser unit 640 and the decompression unit 630 can run on the VLIW processor 610 according to a fixed schedule. For instance, the VLIW processor 610 executes instructions in the preparser unit 630 for a first fixed amount of time and then switches to executing instructions in the decompression unit 640 for a second fixed amount of time. In an alternate embodiment, the decompression unit 630 and the preparser unit 630 can be controlled by an interrupt procedure. For example, when there is a DCT block in the decoded data buffer 770, an interrupt is activated and causes the VLIW processor 610 to stop executing instructions in the preparser unit 630 and to start executing instructions in the decompression unit 630 for a particular amount of time.

In an embodiment, the decoded data buffer 770 stores a macro block (or six DCT blocks) of digital video data that has been decoded by the variable length decoder unit 620. In particular, the decoded data buffer 770 stores the DC coefficients (compressed) and the AC coefficients (compressed) necessary for the inverse discrete cosine transform (IDCT). In an embodiment, the IDCT & IQ unit 775 of the VLIW processor 610 executes software instructions which decompress the digital video data

by performing the inverse quantization (IQ) on a macro block of digital video data at a time. Moreover, the IDCT & IQ unit 775 of the VLIW processor 610 executes software instructions which decompress the digital video data by performing the inverse discrete cosine transform (IDCT) on a macro block of digital video data at a time. The de-shuffling unit 780 can determine the correct macro block position for each macro block on the frame of digital video data by using a macro block index.

The data streamer 705 transfers the digital video data from the IDCT & IQ unit 775 of the VLIW processor 610 to the frame buffer 670 from which a frame of the digital video data can be readily displayed on an electronic display device 120 (Figure 1A). The data streamer 705 is controlled by the de-shuffling unit 780 to ensure the macro blocks are transferred to the correct macro block position on the frame of the digital video data, which is analogous to putting together a jigsaw puzzle. It should be understood that MPEG formatted data does not require de-shuffling.

Figure 8 illustrates a recovered data buffer 750 of Figure 7 in accordance with an embodiment of the present invention. As illustrated in Figure 8, the recovered data buffer 750 includes a first recovered data buffer 805 and a second recovered data buffer 810. In an embodiment, the first recovered data buffer 805 and the second recovered data buffer 810 are each configured to store a segment of digital video data. This implementation facilitates concurrent execution of preparsing of the digital video data by the preparser unit 640 and decoding of the digital video data by the variable length decoder unit 620. It should be understood that the recovered data buffer 750 can include

more than two recovered data buffers. The number of recovered data buffers depends on the performance of the data streamer and available memory resources.

For example, the preparser unit 640 preparses a first segment of digital video data. The first segment of digital video data which has been preparsed is stored in the second recovered data buffer 810. While the preparser unit 640 preparses a second segment of digital video data and fills the first recovered data buffer 805 with the second segment of digital video data, the variable length decoder unit 620 decodes the first segment of digital video data which has been preparsed by emptying the second recovered data buffer 810.

Figure 9 illustrates a decoded data buffer 770 of Figure 7 in accordance with an embodiment of the present invention. As illustrated in Figure 9, the decoded data buffer 770 includes a first decoded data buffer 905 and a second decoded data buffer 910. In an embodiment, the first decoded data buffer 905 and the second decoded data buffer 910 are each configured to store a macro block of digital video data. This implementation facilitates concurrent execution of decoding of the digital video data by the variable length decoder unit 620 and decompressing of the digital video data by the decompression unit 630. It should be understood that the decoded data buffer 770 can include more than two decoded data buffers. The number of decoded data buffers depends on the performance of the data streamer and available memory resources.

For example, the variable length decoder unit 620 decodes a first macro block of digital video data, by decoding a DCT block at a time. The first macro block of digital video data which has been decoded is stored in the second decoded data buffer 910, whereas the data streamer 705 transfers the first macro block of digital video data to the second decoded data buffer 910. While the decompression unit 630 decompresses the first macro block of digital video data, which has been decoded, by emptying the second decoded data buffer 910, the variable length decoder unit 620 decodes a second macro block of digital video data (by decoding a DCT block at a time) and the data streamer 705 fills the first decoded data buffer 905. Moreover, the decompression unit 630 de-shuffles the first macro block.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

CLAIMS

What is Claimed is:

1. A method of processing digital video data for displaying, said method comprising the steps of:

a) preparsing said digital video data to recover a decoding order of said digital video data;

b) decoding a variable length coding format of said digital video data;

c) moving said digital video data that has been processed by said step b); and

d) decompressing said digital video data to facilitate displaying said digital video data on an electronic display device.

2. A method as recited in Claim 1 further comprising the steps of:

accessing a first plurality of said digital video data that has been processed by said step a); and

performing said step a) on a second plurality of said digital video data while said step b) is performed on said first plurality of said digital video data.

3. A method as recited in Claim 1 further comprising the steps of:

accessing a first portion of said digital video data that has been processed by said step b) and that has been processed by said step c); and

performing said step b) on a second portion of said digital video data while said step d) is performed on said first portion of said digital video data.

4. A method as recited in Claim 1 wherein said step a) and said step d) are performed by a very long instruction word (VLIW) processor.

5. A method as recited in Claim 4 wherein said step b) is performed by a variable length decoding unit, and wherein said step a) and said step d) are performed according to time sharing criteria.

6. A method as recited in Claim 1 further comprising de-shuffling said digital video data to form a frame of said digital video data.

7. A method as recited in Claim 1 wherein said variable length coding format comprises a Huffman code format.

8. A method as recited in Claim 1 wherein said digital video data comprises DV formatted data.

9. A method as recited in Claim 1 wherein said digital video data comprises MPEG formatted data.

10. A computer-readable medium comprising computer-executable instructions for performing a method of processing digital video data for displaying, said method comprising the steps of:

a) preparsing said digital video data to recover a decoding order of said digital video data;

b) decoding a variable length coding format of said digital video data;

c) moving said digital video data that has been processed by said step b); and

d) decompressing said digital video data to facilitate displaying said digital video data on an electronic display device.

11. A computer-readable medium as recited in Claim 10 further comprising the steps of:

accessing a first plurality of said digital video data that has been processed by said step a); and

performing said step a) on a second plurality of said digital video data while said step b) is performed on said first plurality of said digital video data.

12. A computer-readable medium as recited in Claim 10 further comprising the steps of:

accessing a first portion of said digital video data that has been processed by said step b) and that has been processed by said step c); and

performing said step b) on a second portion of said digital video data while said step d) is performed on said first portion of said digital video data.

13. A computer-readable medium as recited in Claim 10 wherein said step a) and said step d) are performed by a very long instruction word (VLIW) processor.

14. A computer-readable medium as recited in Claim 13 wherein said step b) is performed by a variable length decoding unit, and wherein said step a) and said step d) are performed according to time sharing criteria..

15. A computer-readable medium as recited in Claim 10 further comprising de-shuffling said digital video data to form a frame of said digital video data.

16. A computer-readable medium as recited in Claim 10 wherein said variable length coding format comprises a Huffman code format.

17. A computer-readable medium as recited in Claim 10 wherein said digital video data comprises DV formatted data.

18. An apparatus for processing digital video data for displaying, said apparatus comprising:

a processor configured to preparse said digital video data to recover a decoding order of said digital video data; and

a variable length decoding unit coupled to said processor, wherein said variable length decoding unit is configured to decode a variable length coding format of said digital video data.

19. An apparatus as recited in Claim 18 wherein said variable length decoding unit accesses a first plurality of said digital video data that has been processed by said processor, and wherein said processor preparses a second plurality of said digital video data while said variable length decoding unit decodes said first plurality of said digital video data.

20. An apparatus as recited in Claim 18 wherein said processor is further configured to decompress said digital video data to facilitate displaying said digital video data on an electronic display device after said variable length decoding unit decodes said digital video data.

21. An apparatus as recited in Claim 20 further comprising a direct memory access (DMA) unit coupled to said processor and coupled to said variable length decoding unit, wherein said DMA unit is configured to transfer said digital video data between said processor and said variable length decoding unit, and wherein said processor accesses a first portion of said digital video data that has been processed by said variable length decoding unit, and wherein said variable length decoding unit decodes a second portion of said digital video data while said processor decompresses said first portion of said digital video data.

22. An apparatus as recited in Claim 18 wherein said processor de-shuffles said digital video data to form a frame of said digital video data after decompressing said digital video data.

23. An apparatus as recited in Claim 18 wherein said processor includes a first recovered data buffer for storing said digital video data after said processor preparses said digital video data.

24. An apparatus as recited in Claim 23 wherein said processor includes a second recovered data buffer for storing said digital video data after said processor preparses said digital video data, and wherein one of said first and second recovered data buffers is filled with said digital video data preparsed by said processor while one of said first and second recovered data buffers is emptied as said digital video data is decoded by said variable length decoding unit.

25. An apparatus as recited in Claim 18 wherein said processor includes a first decoded data buffer for storing said digital video data after said variable length decoding unit decodes said digital video data.

26. An apparatus as recited in Claim 25 wherein said processor includes a second decoded data buffer for storing said digital video data after said variable length decoding unit decodes said digital video data, and wherein one of said first and

second decoded data buffers is filled with said digital video data decoded by said variable length decoding unit while one of said first and second decoding data buffers is emptied as said digital video data is decompressed by said processor.

27. An apparatus as recited in Claim 18 wherein said processor comprises a very long instruction word (VLIW) processor.

28. An apparatus as recited in Claim 18 wherein said variable length coding format comprises a Huffman code format.

29. An apparatus as recited in Claim 18 wherein said digital video data comprises DV formatted data.

30. A digital video data decoder comprising:

a first memory buffer configured to store digital video data received from a source;

a processor coupled to said first memory buffer and configured to preparse said digital video data to recover a decoding order of said digital video data;

a variable length decoding unit coupled to said processor, wherein said variable length decoding unit is configured to decode a variable length coding format of said digital video data; and

a second memory buffer coupled to said processor and configured to store said digital video data after said digital video data is processed by said processor and said variable length decoding unit.

31. A digital video data decoder as recited in Claim 30 wherein said variable length decoding unit accesses a first plurality of said digital video data that has been processed by said processor, and wherein said processor preparses a second plurality of said digital video data while said variable length decoding unit decodes said first plurality of said digital video data.

32. A digital video data decoder as recited in Claim 30 wherein said processor is further configured to decompress said digital video data to facilitate displaying said digital video data on an electronic display device after said variable length decoding unit decodes said digital video data.

33. A digital video data decoder as recited in Claim 32 wherein said processor accesses a first portion of said digital video data that has been processed by said variable length decoding unit, and wherein said variable length decoding unit decodes a second portion of said digital video data while said processor decompresses said first portion of said digital video data.

34. A digital video data decoder as recited in Claim 30 wherein said processor de-shuffles said digital video data to form a frame of said digital video data

after decompressing said digital video data, and wherein said frame of said digital video data is stored in said second memory buffer.

35. A digital video data decoder as recited in Claim 30 wherein said processor comprises a very long instruction word (VLIW) processor.

36. A digital video data decoder as recited in Claim 30 wherein said variable length coding format comprises a Huffman code format.

37. A digital video data decoder as recited in Claim 30 wherein said digital video data comprises DV formatted data.

IMPLEMENTATION OF A DV VIDEO DECODER WITH A VLIW PROCESSOR AND A VARIABLE LENGTH DECODING UNIT

ABSTRACT OF THE INVENTION

A decoder for decoding a plurality of digital video data is described. In an embodiment, the decoder comprises a DV video decoder for decoding digital video data which is formatted according to the DV standard. The DV video decoder has a Very-Long Instruction Word (VLIW) processor and a variable length decoding unit. The VLIW processor includes a preparser unit for recovering a decoding order of the digital video data so that the variable length decoding unit can process the digital video data. The variable length decoding unit decodes a variable length coding format of the digital video data which has been preparsed by the VLIW processor. Furthermore, the VLIW processor includes a decompression unit for decompressing the digital video data which has been decoded by the variable length decoding unit. In an embodiment, the VLIW processor and the variable length decoding unit are formed on the same semiconductor device.

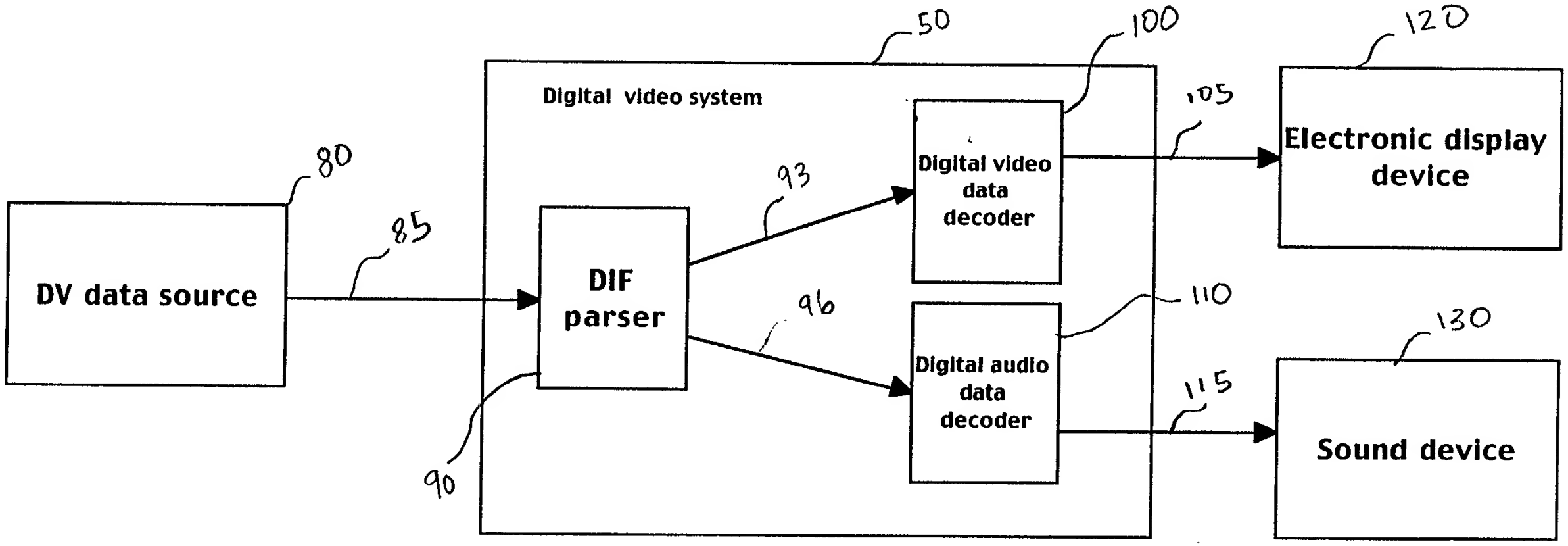
50
Digital video system
100
120
105
Electronic display device
80
85
DV data source
DIF parser
93
Digital video data decoder
96
110
Digital audio data decoder
115
130
Sound device
90

Figure 1A

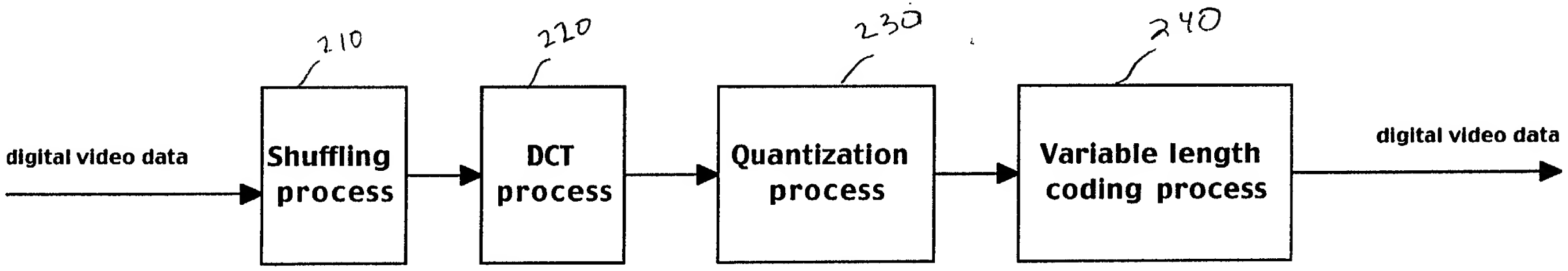

Figure 1B

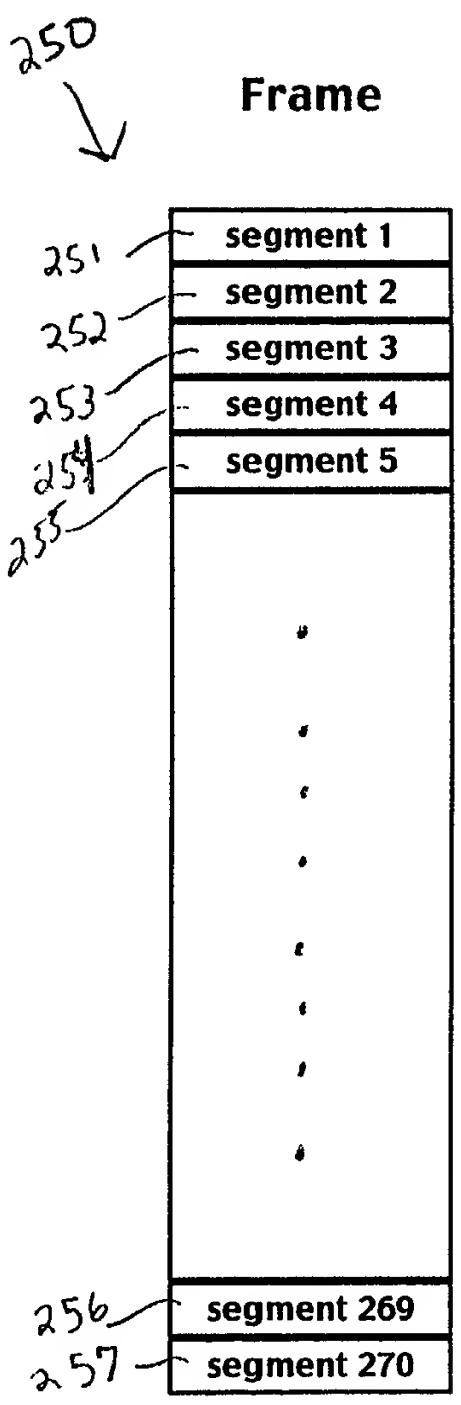

Figure 2

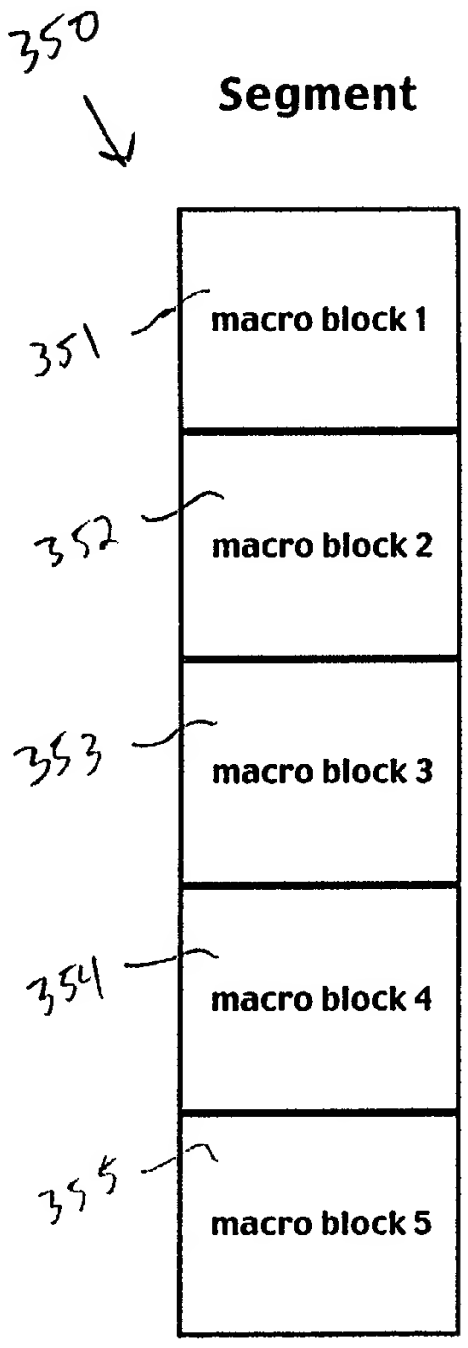

Figure 3

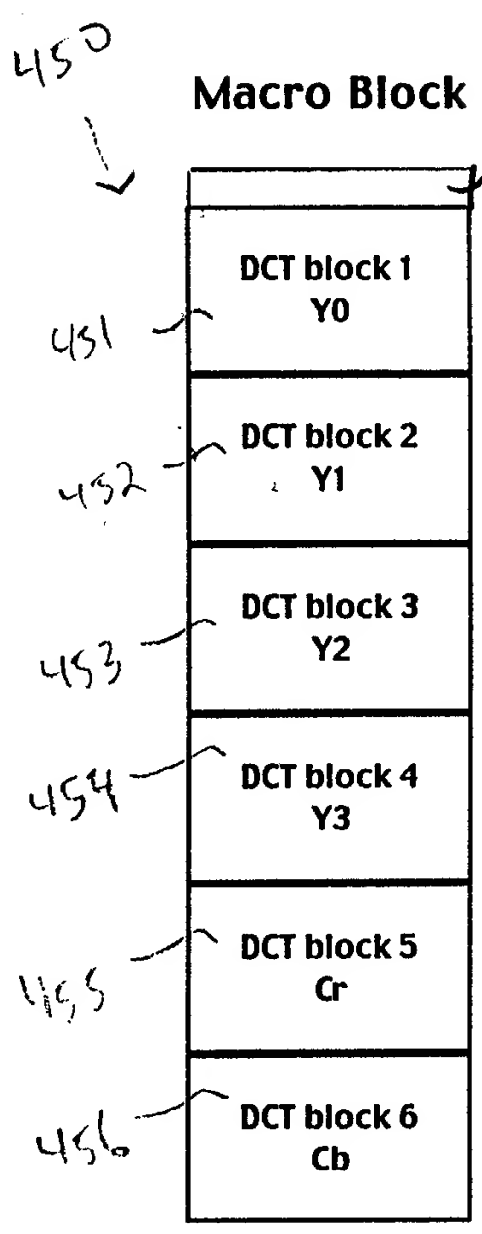

Figure 4

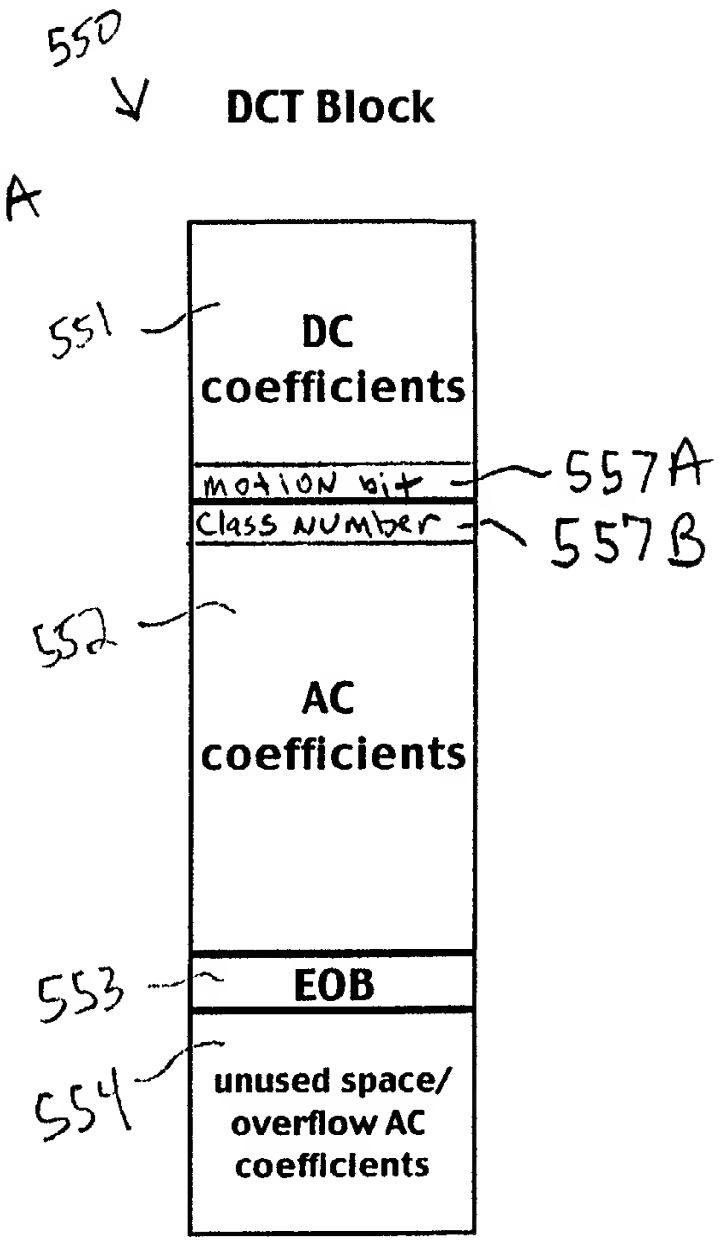

Figure 5

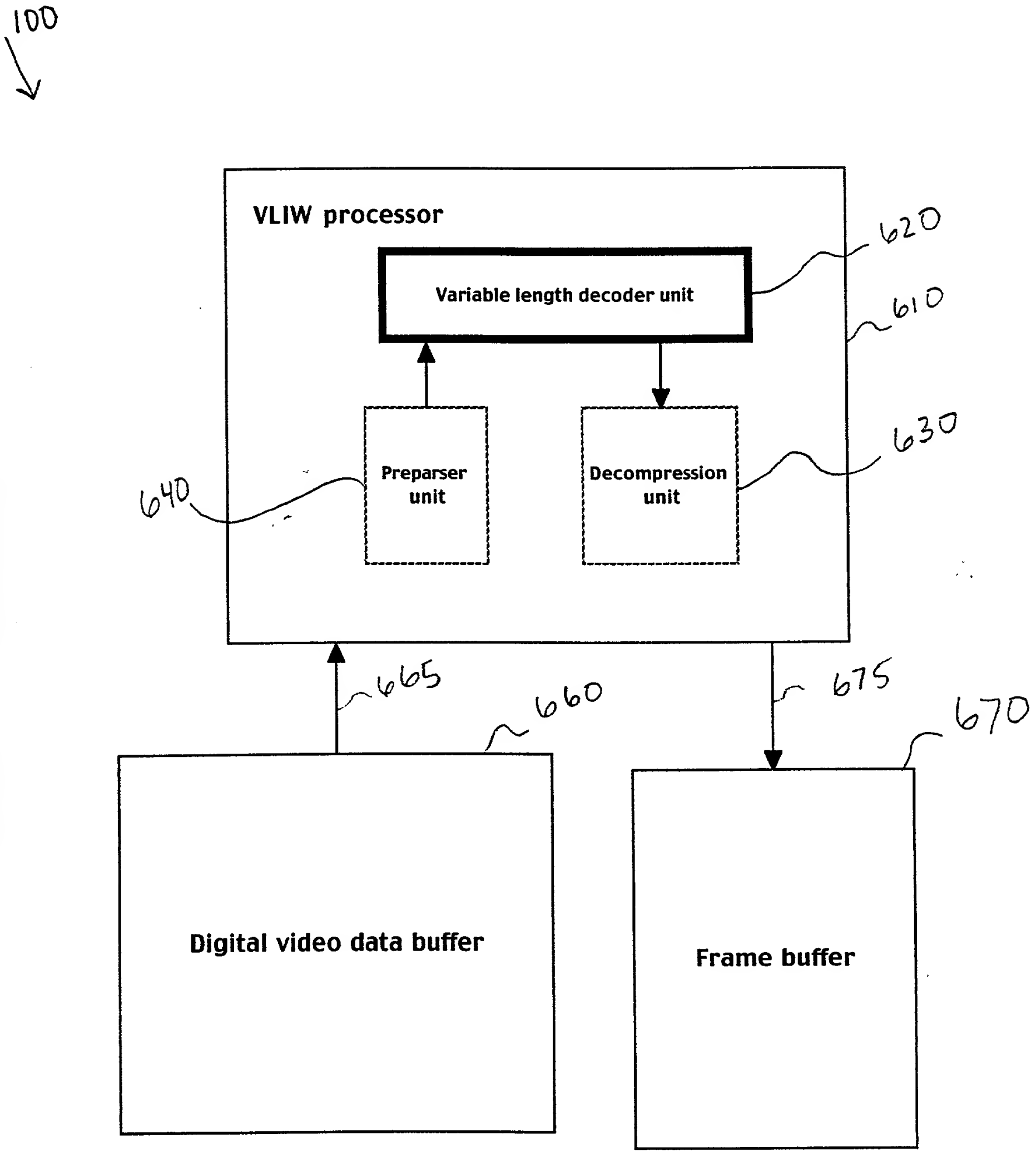
100
VLIW processor
620
Variable length decoder unit
610
630
640
Preparser unit
Decompression unit
665
660
675
670
Digital video data buffer
Frame buffer

Figure 6

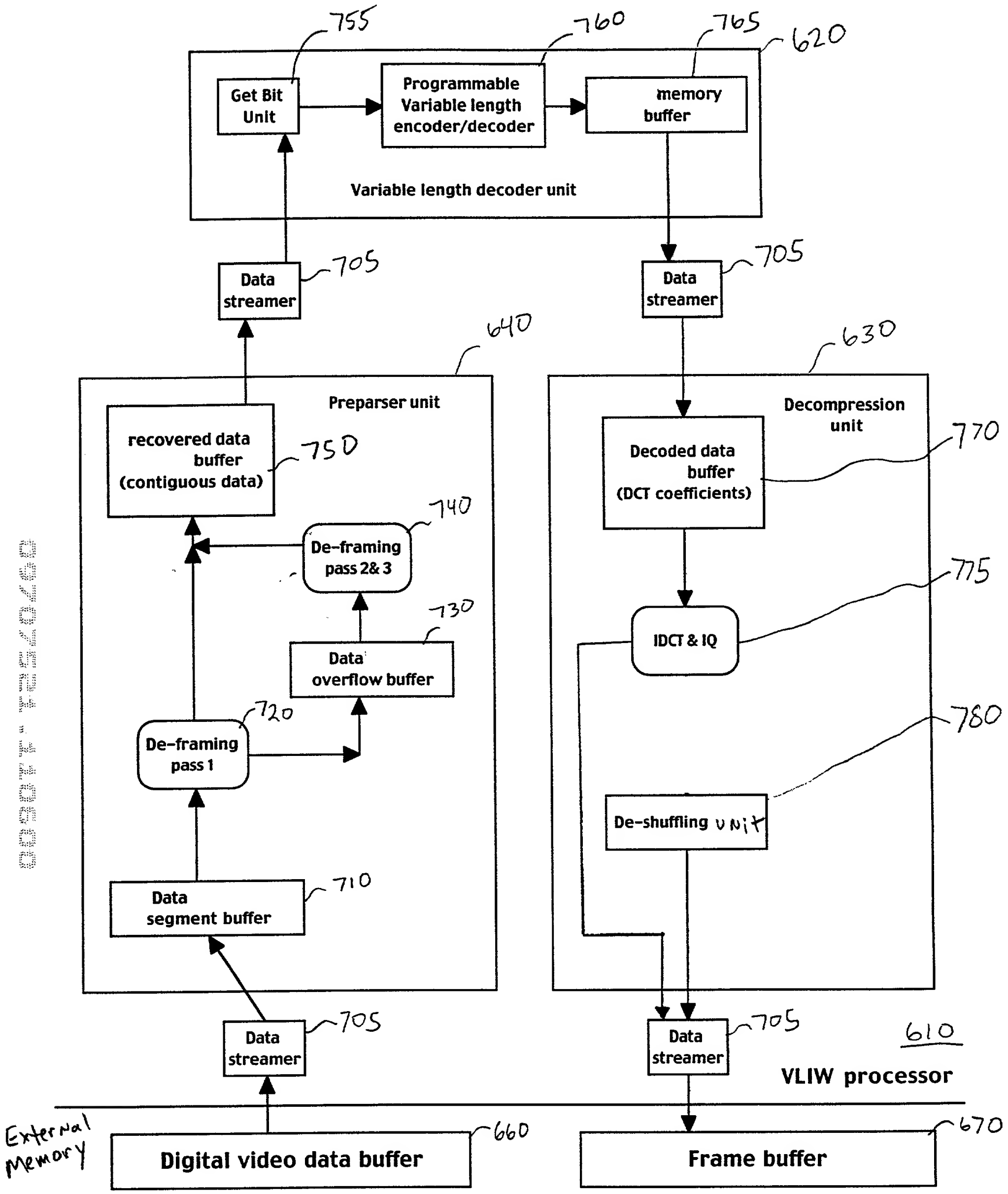
755
760
765
620
Get Bit Unit
Programmable Variable length encoder/decoder
memory buffer
Variable length decoder unit
Data streamer
705
Data streamer
705
640
630
Preparser unit
Decompression unit
recovered data buffer (contiguous data)
750
Decoded data buffer (DCT coefficients)
770
740
De-framing pass 2& 3
775
730
Data overflow buffer
IDCT & IQ
720
780
De-framing pass 1
De-shuffling unit
710
Data segment buffer
Data streamer
705
Data streamer
705
610
VLIW processor
External Memory
660
Digital video data buffer
670
Frame buffer

Figure 7

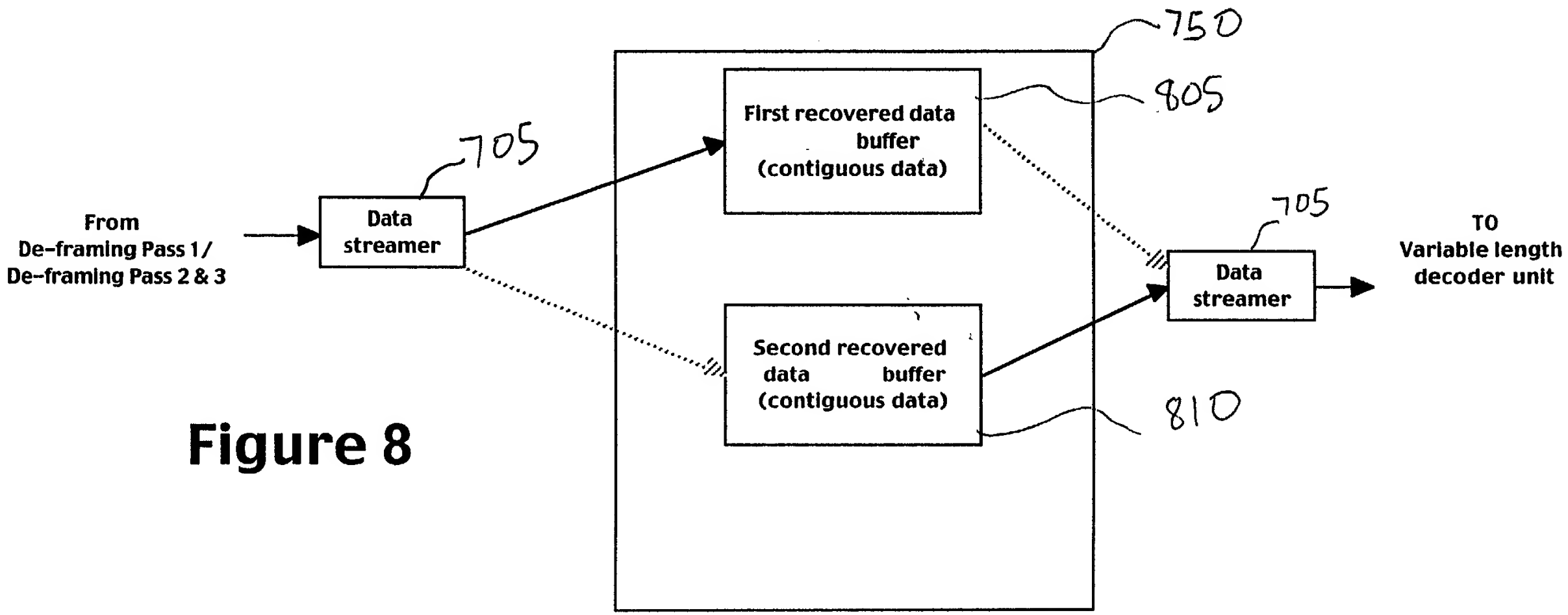

Figure 8

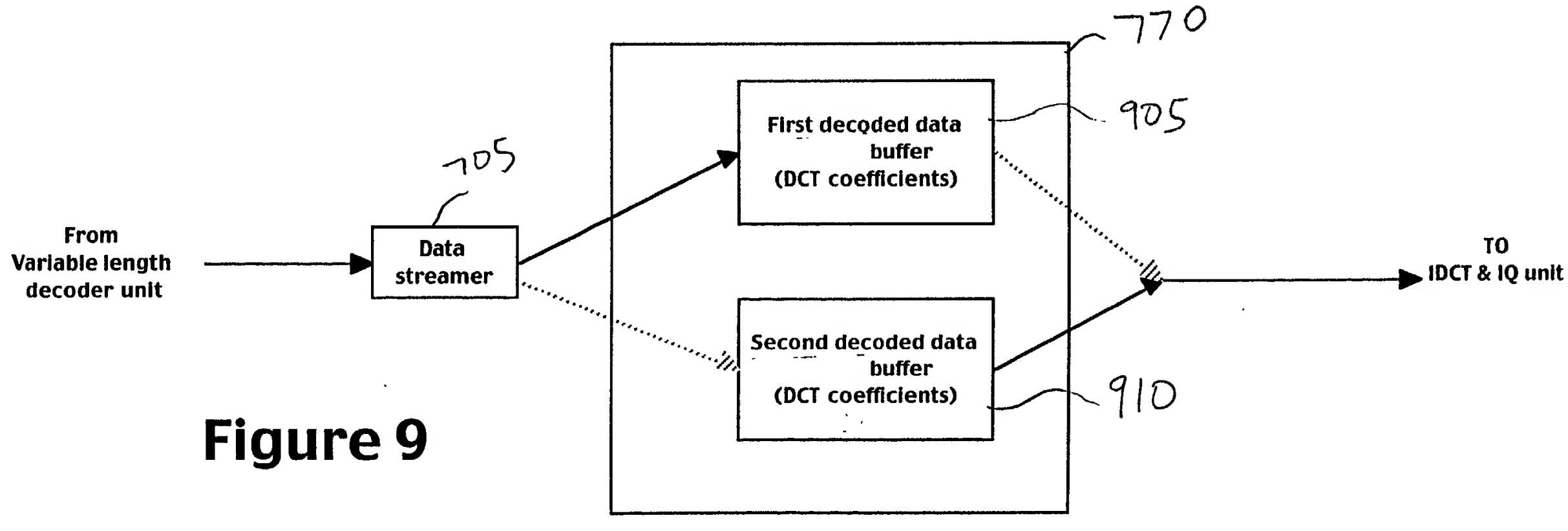

Figure 9

Attorney Docket No.: SONY-50P3845

Declaration and Power of Attorney for a Patent Application

Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

IMPLEMENTATION OF A DV VIDEO DECODER WITH A VLIW PROCESSOR AND A VARIABLE LENGTH DECODING UNIT

the specification of which:

X is attached hereto, or
_____ was filed on _____ as application serial no. _____ : and
_____ was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

Foreign Priority Claim

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Number	Country	Date Filed	Priority Claimed	
			yes	no
			yes	no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)
60/176,256	01/15/00	PENDING

Power of Attorney

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent Trademark Office connected therewith.

James P. Hao	Registration No.: 36,398
Anthony C. Murabito	Registration No.: 35,295
John P. Wagner	Registration No.: 35,398
Glenn D. Barnes	Registration No.: 42,293
Rick G. Brewster	Registration No.: 35,077
Thomas M. Catale	Registration No.: 46,434
Jose S. Garcia	Registration No.: 43,628
Kenneth N. Glass	Registration No.: 42,587
Lin C. Hsu	Registration No.: 46,315
Patrick W. Ma	Registration No.: 44,215
Ronald M. Pomerenke	Registration No.: 43,009
John F. Ryan	Registration No.: P-47,050
William A. Zarbis	Registration No.: 46,120

Send Correspondence to:

WAGNER, MURABITO & HAO LLP
Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060

Signatures

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: **Amelia C. Luna**

Inventor's Signature _____ Date 10/17/2000

Residence San Jose, ~~California~~ Citizenship ~~Philippines~~ USA
(City State)

P.O. Address 6553 Edgebrook Court, San Jose, California 95120

Full Name of Second/Joint Inventor: **Jason (Naxin) Wang**

Inventor's Signature x Naxin Jason Wang Date x 10/17/2000

Residence San Jose, California Citizenship P. R. China
(City State)

P.O. Address 1238 Oregold Place, San Jose, California 95131

rev 2/00 kgr